CHAMP
Chicago side

Eric Oberla

Electronics Godparent Review 10/5/2010

structure

- Full DLL (delay locked loop)
- DLL test structure
- Ring oscillator
- Transmission Lines
- Resistors

Structure/test plans

- Full DLL (delay locked loop)
- DLL test structure -- joint UC/UH eval board
- Ring oscillator (december)
- Transmission Lines – probe pads
- Resistors -- probe pads

DLL

- On-chip, analog DLL will allow us to have a better controlled sampling rate.
- Provide us a cleaner sampling window
- No dead zone of sampling (if the effective delay free running delay line is less than the period of the input clock -> dead time)

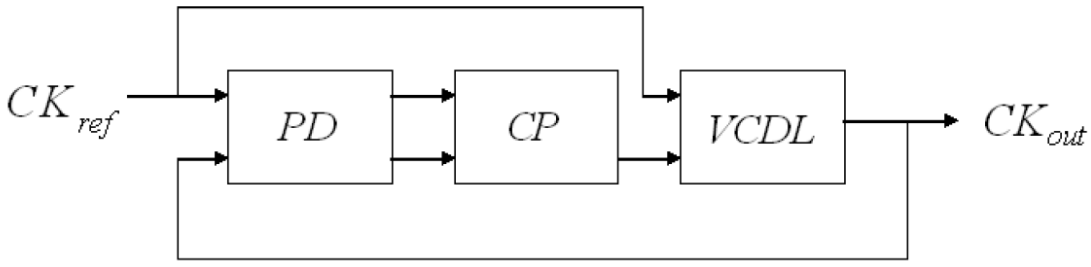
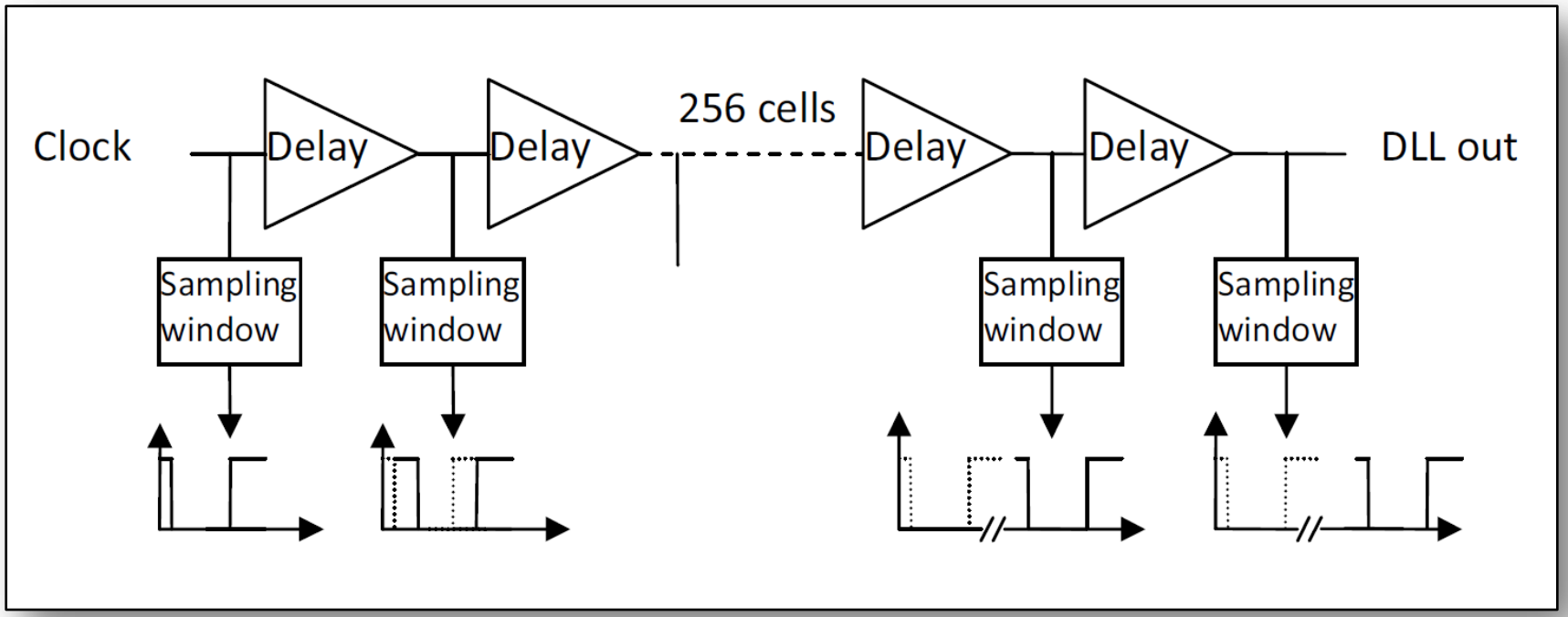


Figure 1-1 Simplified block diagram of a DLL

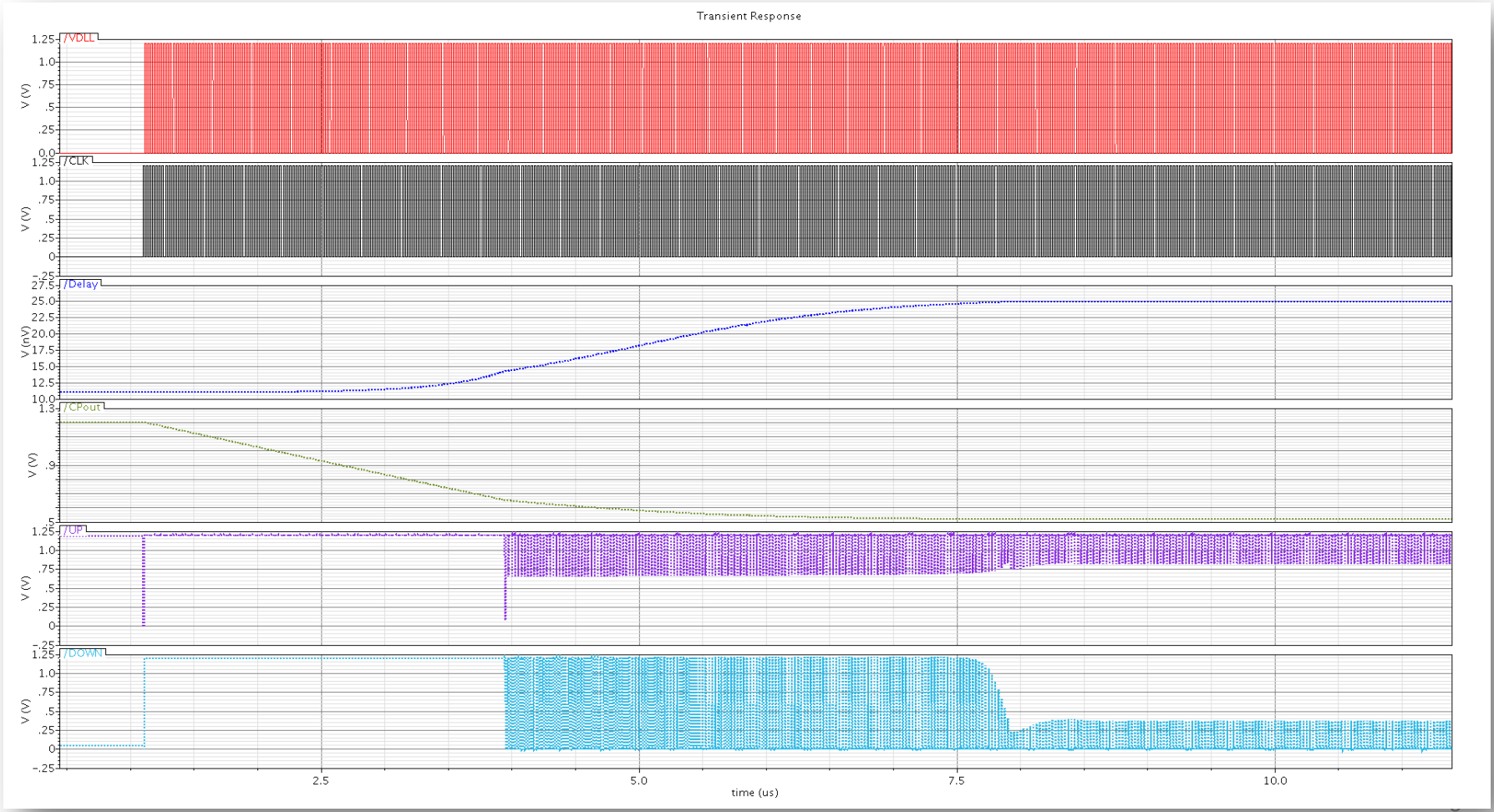
DLL - principle

- Delay line structure: chain of small delays.



Generates a sampling frequency equal to $\frac{1}{\text{Delay}}$

DLL simulation success



summary

- Eval board under development
- Testing in December
- Functional DLL + Hawaii side structures (DACs, SPI, …next talk) should prove useful next design submission

backup

Delay Locked Loop principle

1. VCN and VCP are set to their max value (1.2 & 0 resp.).
   - ✓ The propagation delay in the DLL is then the smallest -> 11ns.
2. The delay is increased until it reaches the delay of one clock cycle.
3. The phase comparator locks then the delay of the delay line at one clock cycle